VALPARAISO UNIVERSITY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ECE 221 **COURSE SYLLABUS** **FALL 2003**

Title and Credit:	Digital System Design	3 credits
Time and Place:	Lecture: 12:55 p.m. - 1:45 p.m. MWF Lab BX: 8:30 a.m. - 11:00 a.m. T Lab CX: 2:00 p.m. - 4:30 p.m. T	Room 131 Gellersen Center Room 185 Gellersen Center Room 185 Gellersen Center
Course Instructors:	Eric W. Johnson Office: 137 Gellersen Center Phone: 464-5176 Office Hours: MWF 2:00-3:00pm email: eric.johnson@valpo.edu WWW: http://diamond.gem.valpo.edu/~ejohnson	

Required Materials:

Text:	Allen Dewey, Analysis and Design of Digital Systems with VHDL, PWS Publishing Company, 1997, 682 pages, ISBN 0-8053-2703-7.
Software:	Mentor Graphics Software Tool Suite (Sun Workstations)
Web Site:	Located through CourseVU (http://coursevu.valpo.edu)

Course Description: This course is designed to give students an introduction to digital concepts, including the analysis and design of combinational and sequential digital circuits. It provides a foundation for subsequent study of computer architecture and design.

Instructional Objectives: Once you've completed this course, you should be able to:

- Convert values between decimal, binary, hexadecimal and octal number systems.
- Perform arithmetic operations on binary, hexadecimal and octal number systems.
- Design minimized combinational logic circuits using Karnaugh Maps or Espresso given natural language descriptions or truth table representations.
- Implement combinational circuits using simple gates, complex gates, steering logic, programmable logic or universal gates.
- Given a set of input waveforms, sketch the output waveforms for various memory types (SR, JK, D, and T) and element classifications (latch, gated latch, and edge-triggered flip flop)
- Create a minimized finite state machine given natural language descriptions or state diagram representations.
- Implement (create, verify and debug) digital designs using integrated circuits both standard off-the-shelf parts and PALs.

Throughout the semester, I will hand out more detailed lists of concepts that I feel you should know at the end of each section (sectional objectives). Exams will cover material directly from these objectives.

Topical Outline:

1. Introduction to Digital Design and Number Systems
2. Combinational Logic Design
3. Sequential Logic Design

Homework: Homework assignments are to be written on 8-1/2" x 11" paper, one side only, and not folded. Sheets should be stapled together in the upper left-hand corner with the cover sheet on top. All homework is due at the beginning of the class period on the date the homework is due (see course

schedule). Late homework (including assignments turned in at the end of the class period on the due date) will be deducted as follows:

25% off - during the class period they are due (5 minute grace period)
50% off - 1 school day late
No Credit - 2 or more school days late

Late homework will be accepted only with a **pre-approved valid written** (email included) excuse (illness or family crisis are generally valid while the network being down is not valid). No credit will be given for any late assignments turned in after the graded papers are returned.

Design Projects: Larger design projects will be assigned throughout the semester to build on the basic concepts described in the lectures and supplement the homework assignments. Final versions will be done using the Mentor Graphics software tools. All design projects are due at the beginning of the class except where noted. The same late penalty as homework assignments applies to design projects.

Laboratories: Laboratories will be performed every other week at the times listed on the first page. A lab handout will be given at the first lab session describing lab policies and procedures. Your lab grade will be a combination of your attendance and your submitted lab reports.

Examinations: Two comprehensive exams will be given in Room 136 Gellersen on the following dates:

Exam #1	Wednesday October 1, 2003
Exam #2	Wednesday November 12, 2003

These exams will be given during the class period. A review session may be scheduled before the exam to discuss any questions about the material covered by the exam.

Grading:	Homework (lowest score dropped)	10%
	Design Projects	15%
	Exams	30%
	Laboratories	20%
	Final Examination	25%

Course grades are guaranteed for the following final percentages:

93% or higher	A	90% or higher	A-
87% or higher	B+	83% or higher	B
80% or higher	B-	77% or higher	C+
73% or higher	C	70% or higher	C-
67% or higher	D+	63% or higher	D
60% or higher	D-	below 60%	F

If there are any borderline percentages, I reserve the right to adjust grades based on the following factors: attendance, the upward/downward trend in test and design project grades, and/or your participation in class. You will be able to observe your current grade online using the coursevu online grade book which can be accessed through the course home page.

Course Policies: Regular attendance in the classroom is expected. If you miss class for any reason, it is your responsibility to turn in assignments on time and get notes you may have missed from someone in the class. There may be in-class projects (ICPs) performed during some class periods. You will not be able to make up those ICPs unless you have a **pre-approved valid written excuse** for your absence.

The course will be conducted under the Valparaiso University Honor Code. All assignments are to be performed and documented individually by each student. A list of examples on what is considered

authorized and unauthorized aid is given below. If you have any questions about this policy, do not assume anything, always ask first.

Authorized Aid:

1. Discussion of a strategy or methodology for solving homework assignments when both students do NOT have a solution worked out.
2. Questions about the understanding or wording of a problem.
3. Questions concerning the Sun workstations or how to use the computer-aided design tools (Mentor Graphics).
4. Any aid obtained from the professor is obviously authorized, and will generally be shared with all other students, either through the WWW or by electronic mail.

Unauthorized Aid:

1. Detailed discussions of assignment solutions or studying another student's solution (including design schematics or waveforms in Mentor Graphics).
2. Copying (electronic or otherwise) of assignments or projects in whole or in part from anyone in the current class or in previous classes.
3. Using another persons Sun Workstation account for design projects or homework assignments.
4. Any communication between students during an exam or quiz.

ECE 221 Tentative Course Outline				
Lesson #	**Date**	**Topics**	**Readings**	**Assignment**
1	Aug. 27 (W)	Course Handouts, Intro. to Digital Design	Chapter 1	
2	Aug. 29 (F)	Digital Design Process	Chapter 1	
3	Sept. 1 (M)	Binary Numbers and Binary Conversions	2.1 - 2.4	HW #1
4	Sept. 3 (W)	Octal and Hexadecimal Number Systems	2.4 - 2.8	
5	Sept. 5 (F)	Binary Operations	3.1 - 3.5	HW #2
6	Sept. 8 (M)	Combinational System Analysis	3.6 - 3.8	
7	Sept. 10 (W)	Canonical Forms and Documentation	3.8 - 3.10	HW #3
-	Sept. 12 (F)	NO CLASS - LAB ON TUESDAY (Lab #1)		
8	Sept. 15 (M)	Minimization Techniques	4.1 - 4.3	
9	Sept. 17 (W)	Karnaugh Maps	4.4	HW #4
10	Sept. 19 (F)	K-Maps and Don’t Care Conditions	4.4 - 4.5	
11	Sept. 22 (M)	Quine-McCluskey Technique	4.5 - 4.7	HW #5
12	Sept. 24 (W)	Espresso	-	DP #1
-	Sept. 26 (F)	NO CLASS - LAB ON TUESDAY (Lab #2)		
13	Sept. 29 (M)	Two-Level Networks	5.1 - 5.2	

-	Oct. 1 (W)	EXAMINATION #1 (Chapters 1-4)		
14	Oct. 3 (F)	Steering Logic	5.2 - 5.3	HW #6
15	Oct. 6 (M)	Multiplexers (ICP)	5.4	
16	Oct. 8 (W)	Decoders and Memory	5.5 - 5.6	DP #2
-	Oct. 10 (F)	NO CLASS - LAB ON TUESDAY (Lab #3)		
17	Oct. 13 (M)	Programmable Logic Devices	5.7	HW#7
18	Oct. 15 (W)	Adder and ALU Circuits	-	
-	Oct. 17 (F)	NO CLASS - FALL BREAK		
19	Oct. 20 (M)	Multiplier Circuits	-	
20	Oct. 22 (W)	Sequential System Overview	8.1	DP #3
-	Oct. 24 (F)	NO CLASS - LAB ON TUESDAY (Lab #4)		
21	Oct. 27 (M)	Memory Elements	8.2	
22	Oct. 29 (W)	Literal Analysis of Sequential Systems (ICP)	8.3	HW #8
23	Oct. 31 (F)	Symbolic Analysis of Sequential Systems	8.4	
24	Nov. 3 (M)	Timing Issues	8.5	HW #9
25	Nov. 5 (W)	Registers, Shift Registers	10.2 - 10.3	DP #4
-	Nov. 7 (F)	NO CLASS - LAB ON TUESDAY (Lab #5)		
26	Nov. 10 (M)	Counters and Exam Preview	10.3 - 10.4	HW #10
-	Nov. 12 (W)	EXAMINATION #2 (Chapters 1-8)		
27	Nov. 14 (F)	Exam Review and Design Project #5 Info	-	
28	Nov. 17 (M)	Counter Design (ICP)	10.4	
29	Nov. 19 (W)	Finite State Machines	9.1 - 9.2	DP #5
-	Nov. 21 (F)	NO CLASS - LAB ON TUESDAY (Lab #6)		
THANKSGIVING BREAK				
30	Dec. 1 (M)	Finite State Machines (ICP)	-	
31	Dec. 3 (W)	State Minimization	9.3	HW #11
32	Dec. 5 (F)	State Minimization (ICP)		
33	Dec. 8 (M)	Digital Circuit Fabrication (Video)		

34	Dec. 10 (W)	Course Review and Final Exam Preview		Final Project
-	Dec. 12 (F)	NO CLASS - LAB ON TUESDAY (Lab #7)		
FINAL EXAM - Thursday December 18, 1:00 - 3:00pm				

Fall 2003 Tentative Laboratory Schedule

Date	Experiment Title
Sept. 9	Mentor Graphics Tutorial
Sept. 23	Standard Logic Components
Oct. 7	Digital Logic Minimization
Oct. 21	Programmable Logic Devices
Nov. 4	Sequential Circuits and Logic Analyzer Basics
Nov. 18	Custom Counter Design
Dec. 9	Propagation Delay