

# Propagation Delay in Logic Circuits

ECE 221

Fall 2003

## I. INTRODUCTION

The objectives of this experiment are to show the effects of propagation delay on logic circuit performance and to illustrate the effect of capacitance on a circuit at high frequencies.

## II. PRE-LAB

1. Using Mentor Graphics create the INVERTER chain circuit shown in Figure 1 using the 74LS04 inverter. To accomplish this, you will need to access the inverter component from a **74LS** library not the **gen\_lib**. Make sure you select the inverter that looks like an inverter and not a box.
2. Simulate the INVERTER chain circuit and find the typical propagation delays when the input goes from a low-to-high transition for one inverter.
  - 1). First add the average delay time to the inverter models. Invoke **Analysis** under the **Kernal** option from the **Setup** pull down menu. In the **Setup Analysis** dialog window that appears, click on **Delay** and hit **OK**. This will assign a “typical” delay to each inverter (not worst or best case delay).
  - 2). Add the traces (input and output) and run the simulation.
  - 3). Find the delay between the input and output using cursors.
    - To add a cursor to trace window, place the mouse cursor in the trace window and hold the right mouse button down. Select **Add** under the **Cursors** option. When the **Add Cursors** pop-up window appears, give the cursor a name (C0) and a location (10). Then add another cursor (C1) at location 20. You should see the location of C1 and the difference between C1 and C0 at the bottom of cursor C1.
    - Unselect all of the trace cursors and then choose **Slide/Snap** under the **Cursors** option. Change the cursor movement to **Snap to NEXT EDGE** and hit **OK**.
    - Measure the delay between the rising edge of the input and the rising edge of the output by moving the cursor C0 on the input rising edge and C1 on the output rising edge. To get accurate readings again use the **Slide/Snap** option under the **Cursors** option. Select C0 and then choose the **Slide/Snap** option. Your trace cursor should move around in the trace window as you move your mouse. Move the mouse cursor near the input rising edge and click on the left mouse button. Your trace cursor should snap to that edge. Do the same with C1 and the rising output edge.
  - 4). Given the delay for all six inverters, compute the delay for one inverter.
3. Print out a copy of both the schematic and the waveforms and place them in your lab notebook. At the bottom of the waveforms put the average delay value for one inverter.

## III. PROPAGATION DELAY

1. Create the circuit shown in FIGURE 1 (only one 7404 (hex-inverter) is needed). Make sure the chip has the source voltage and ground applied to the proper pins.

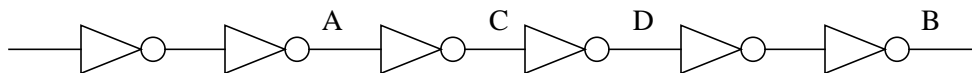


FIGURE 1 - Series INVERTER Circuit

2. Apply a 0 to 5 volt pulse voltage (make sure it is 0 to 5 volts) from the function generator to the beginning inverter in the chain.
3. Display the voltage at the output of the second gate (point A) on one source channel, and display the output from the last gate (point B) on the other channel.
4. Measure the time delay between these two points in the circuit. To find the delay, go to a very high frequency (about 100kHz). Increase the frequency until you can get an accurate measurement for the time delay. Using the midpoint of the waveform transitions, find the delay when the signal transitions from a low value to a high value and when the signal transitions from a high to low value. Find the average of the two values. This result is the propagation delay across four inverters.
5. Answer the following questions in your lab notebook.
  - 1). What is the average propagation or time delay for one logic inverter?
  - 2). Why is there a time delay through each inverter?
  - 3). How does the average propagation delay compare with the typical delay that you found in the prelab? State why these values might be different.

#### IV. EFFECT OF CAPACITANCE

Stray capacitance is present in every logic circuit. Typically, this capacitance can come from at least three different sources.

- Output circuits, including the gate's output transistors, internal wiring, and packaging, have a small amount of capacitance associated with them typically on the order of 2-10 picofarads for many logic families.
- The wiring that connects gates together (the output of one gate to the input of another) has a capacitance of about 1 picofarad per inch depending on the wiring technology.
- Input circuits, like output circuits, also have capacitance associated with internal wiring and packaging ranging from 2 to 15 picofarads per input in a typical logic family.

This capacitance is known as the *capacitive* or *AC load* and can have a significant impact on a circuit's operation.

1. To help illustrate the impact of capacitance on a circuit, connect a 0.01 microfarad capacitor at the output of the third gate (point C to ground). Determine the propagation delay for the inverter that is impacted by the capacitor (the inverter between point C and point D). This can be accomplished by again measuring the delay from point A to point B and then subtracting off the average delay for the other three inverters. How does the propagation delay of the inverter between points C and D compare with the average inverter delay?
2. Measure  $V_C$  on one scope channel and  $V_D$  (the voltage after the fourth inverter) on the other channel. How does the extra capacitor effect these waveforms? Sketch these waveforms in your lab notebook.
3. Increase the frequency until  $V_C$  looks more like a sawtooth wave than a square wave. What happens to the width of the high voltage at point D as the frequency increases? Now measure  $V_A$  and  $V_B$  again. What has happened to the delay between point A and point B? Continue to increase the frequency until the overall series circuit no longer functions correctly. Record that frequency value. Explain why the circuit will not function properly at any frequency higher than your recorded value.
4. Increase the capacitance to 0.1 microfarads and repeat Step 3. From these results what conclusions can you make about of the existence of extra capacitance in a circuit?

## V. LOGIC SYSTEM PERFORMANCE

1. Create the circuit shown in Figure 2 and investigate the consequences of propagation delay. Sketch the expected output of the circuit if all gates were ideal (there was no propagation delay).

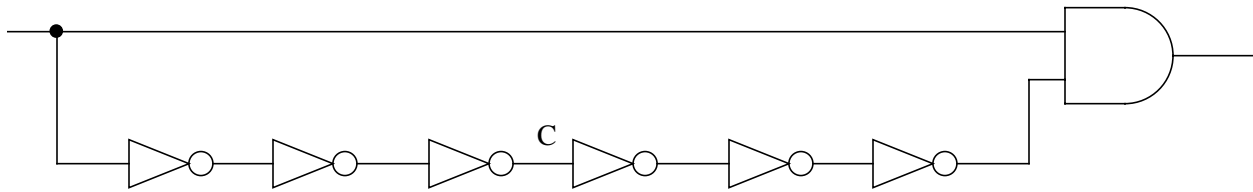


FIGURE 2 - AND/INVERTER Circuit

2. What is the propagation delay through the circuit when the input signal transitions from low value to a high value? (use the midpoint of the waveform to determine the value)
3. Add the 0.1 microfarad capacitor at point C. Again measure the low-to-high transition delay. What happens as the frequency of the source increases?

## VI. SUMMARY and ANALYSIS

In your lab notebook answer all of the questions posed in this handout (you can answer them at the step in the procedure not at the end of the lab) AND then write a paragraph which summarizes what you did in this experiment and the conclusions you obtained.