

# **ECE 221 Digital Logic Design**

## **Sectional Objectives**

### **Section II - Dewey Chapters 1-5, 8, 10.2-10.3**

After reading the above chapters and sections you should be able to:

- represent a combinational expression in the following forms: Sum-of-Products (SOP) Product-of-Sums (POS), minterm list, maxterm list.
- use DeMorgan's theorem to complement a function or convert a function to a new representation.
- use Karnaugh maps to minimize logic expressions in either SOP or POS form.
- use Espresso to minimize logic expressions in either SOP or POS form.
- create a minimized combinational logic expression from a specification (english prose).
- create a minimized implementation of boolean expression using simple gates (AND, OR, INV), complex gates (XOR, XNOR), steering logic (MUX, DECODER), programmable logic (ROM, PLA, PAL) or universal gates (NAND, NOR).
- given a set of input waveforms, sketch the output waveforms for various memory types (SR, JK, D, and T) and memory classifications (latch, gated latch, and edge-triggered flip flop)
- create a state transition table and a state diagram from a sequential system schematic (Mealy or a Moore machine) using literal or symbolic analysis.
- given a sequence of operations, determine the output of a universal shift register after each clock period.

Exam #2 Information:

- Open Book, Closed Note
- 3-4 Problems